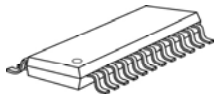
16-Channel SPWM Constant Current LED Driver with Lower Ghosting Effect Elimination

Features

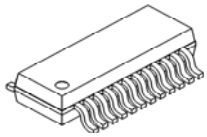
- 16 constant-current output channels
- 16-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- 6-bit programmable output current gain
- Constant output current range:
  1~ 45mA at 5.0V supply voltage
  1~30mA at 3.3V supply voltage
  1~30mA at 5/3.3V supply voltage (GM package)
- Output current accuracy:
  Between channels: <±2.5% (max.), and
  Between ICs: <±3% (max.)
- Integrated lower ghosting effect elimination
- Staggered delay of output, preventing from current surge
- Maximum data clock frequency: 30MHz
- Maximum gray scale clock frequency: 33MHz
  Refresh rate doubled by innovative rising/falling edge trigger GCLK
- Schmitt trigger input
- 3.0V-5.5V supply voltage
- Package MSL Level : 3

Shrink SOP



GP: SSOP24L-150-0.64

Thin Shrink SOP



GM: mSSOP24L-100-0.5

Product Description

MBI5043 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16-bit color depth which features a 16-bit shift register which converts serial input data into each pixel gray scale of output port. The output current can be preset through an external resistor. Moreover, the preset current of MBI5043 can be further programmed to 64 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM) technology, MBI5043 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit color depth video, S-PWM reduces the flickers and improves the fidelity. MBI5043 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5043 drives the corresponding LEDs to the brightness specified by image data. With MBI5043, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED’s brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data. For time-multiplexing LED displays, MBI5043 featured pre-charge to eliminate the lower-ghosting effect induced by parasitic capacitance of the board.

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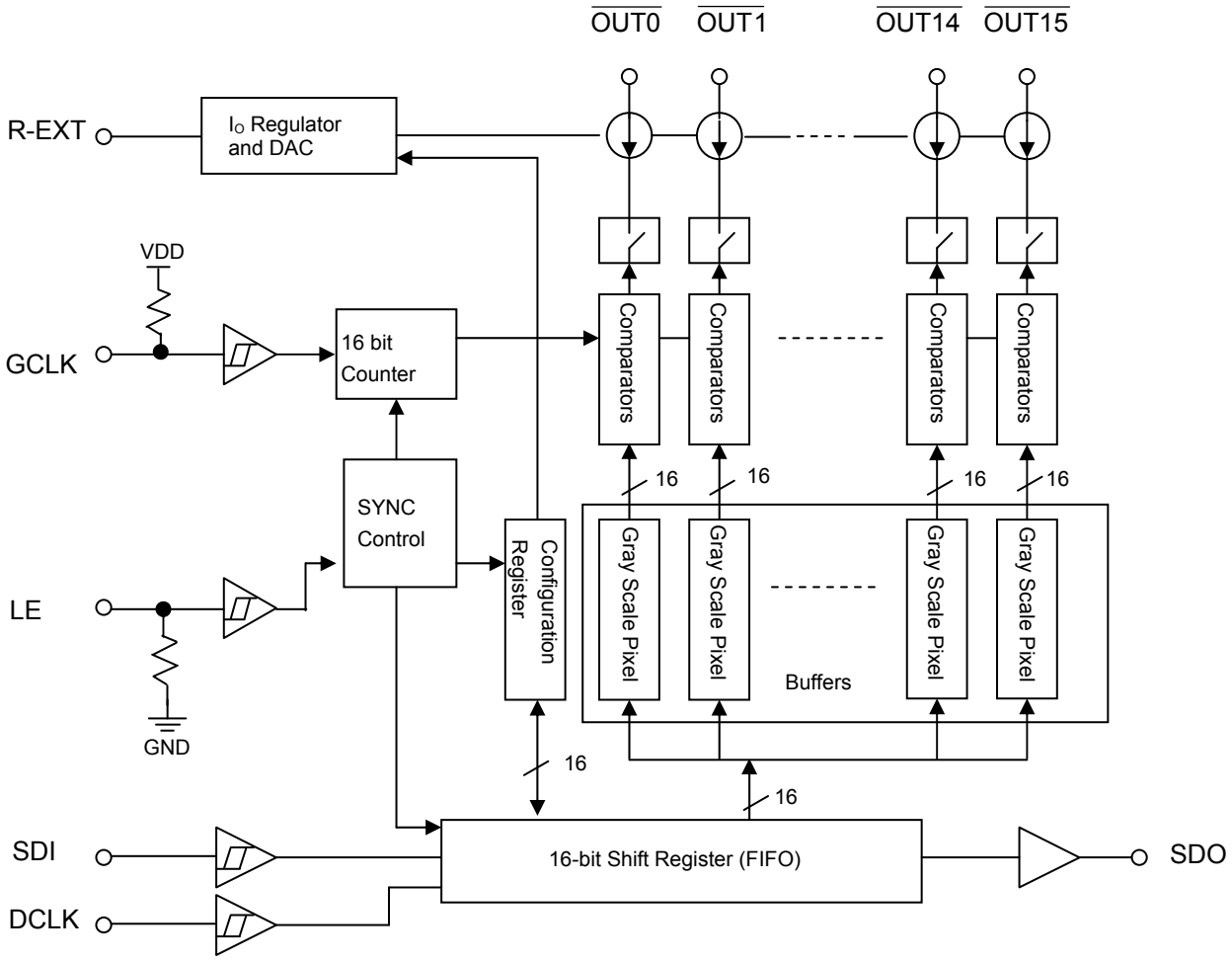
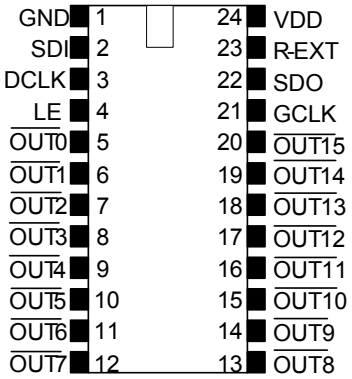
Block Diagram



Pin Configuration



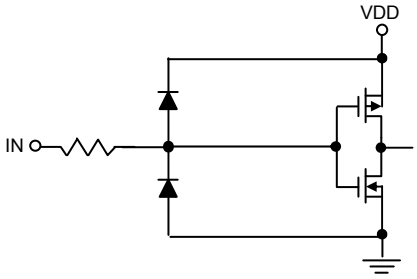
MBI5043GP/GM

Terminal Description

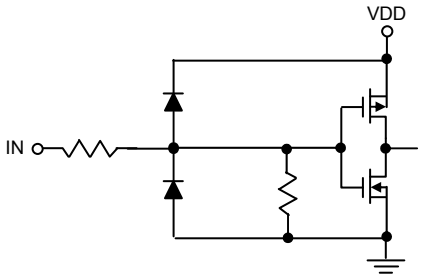
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

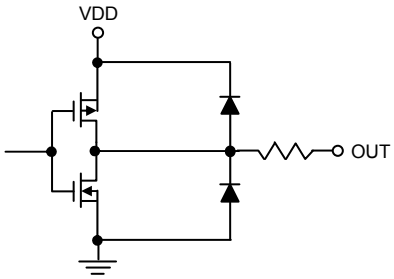
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	-0.5~+7	V
Input Pin Voltage (SDI, CLK, LE, GCLK)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+45	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~+17	V
GND Terminal Current		I_{GND}	+720	mA
Power Dissipation (On PCB, Ta=25°C)*	GP Type	P_D	2.00	W
	GM Type		1.60	
Thermal Resistance (On PCB, Ta=25°C)*	GP Type	$R_{th(j-a)}$	50.00	°C/W
	GM Type		62.00	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 3A (7KV)	-
	Machine Mode (ANSI/ESD S5.2-2009)	MM	Class M4 (450V)	-

* The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested operation temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

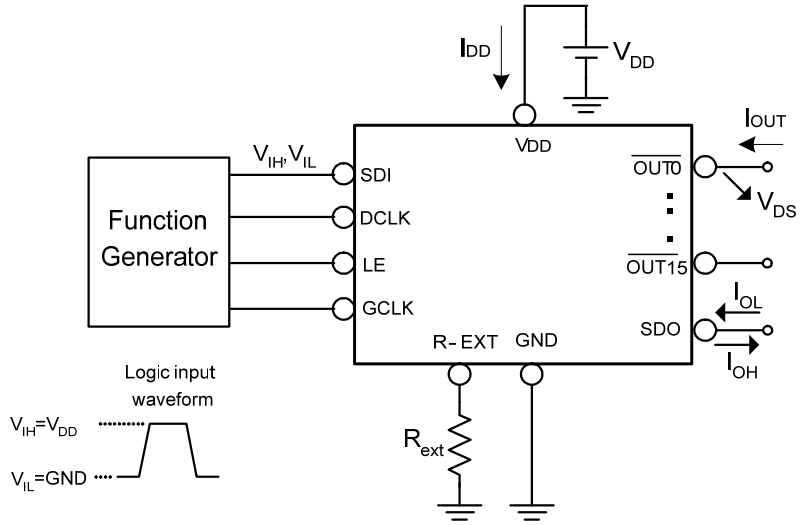
Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@20mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±3.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.0	4.0	mA
		I_{DD}(off) 2	R_{ext}=12KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.0	6.0	
		I_{DD}(off) 3	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.0	8.0	
		I_{DD}(off) 4	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	9.0	12.5	
	"On"	I_{DD}(on) 1	R_{ext}=12KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	4.0	6.0	
		I_{DD}(on) 2	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	6.0	8.0	
		I_{DD}(on) 3	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.5	13.0	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA, V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA, V_{DS}=1.0V	R_{ext}=700Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=700Ω@20mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 3.0V and 3.6V		-	±1.0	±3.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.0	4.0	mA
		I_{DD}(off) 2	R_{ext}=12KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.0	6.0	
		I_{DD}(off) 3	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5.0	7.0	
		I_{DD}(off) 4	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.5	8.5	
	"On"	I_{DD}(on) 1	R_{ext}=12KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	4.0	6.0	
		I_{DD}(on) 2	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	5.5	7.5	
		I_{DD}(on) 3	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.0	9.0	

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1.0V R_L=200Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	7	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		7	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		7	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		7	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	20	25	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	30	60	ns
	LE – SDO**	t_{PD2}		-	30	60	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$ *	t_{DL1}		-	5	8	ns
Pulse Width	LE	$t_{w(L)}$		15	-	-	ns
	DCLK	$t_{w(DCLK)}$		10	-	-	ns
	GCLK	$t_{w(GCLK)}$		10	-	-	ns
	GCLK,2x	$t_{w(GCLK, 2x)}$		15	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	15	25	ns
Output Fall Time of Output Ports		t_{OF}		-	15	25	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency***		F_{GCLK}		-	-	33	MHz
2x Gray Scale Clock Frequency ***		$F_{GCLK, 2x}$		-	-	16.5	MHz

* Refer to the Timing Waveform, where n=0~7

** In timing of “Read Configuration”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

*** With uniform output current.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

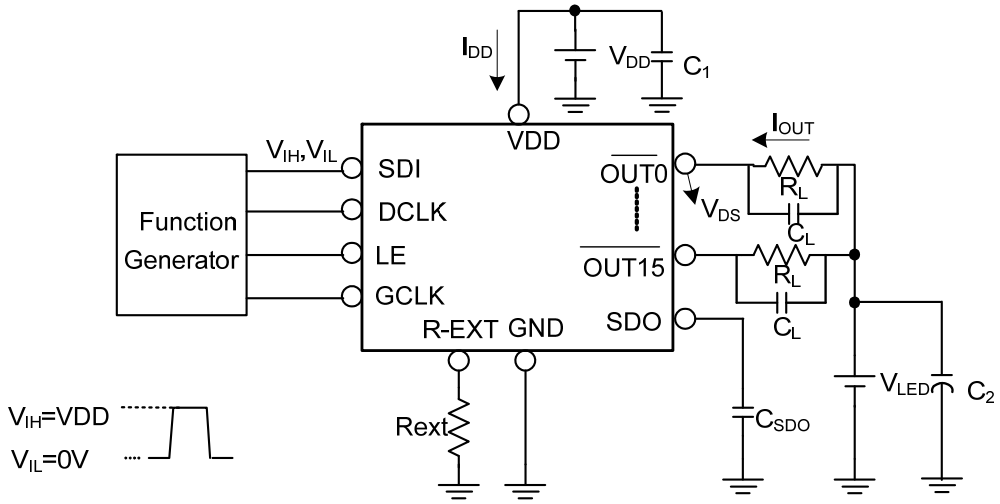
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1.0V R_L=200Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	10	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		10	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		10	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		10	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		10	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25	30	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	50	80	ns
	LE – SDO**	t_{PD2}		-	50	60	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$*	t_{DL1}		-	8	10	ns
Pulse Width	LE	$t_{w(L)}$		20	-	-	ns
	DCLK	$t_{w(DCLK)}$		15	-	-	ns
	GCLK	$t_{w(GCLK)}$		15	-	-	ns
	GCLK,2x	$t_{w(GCLK, 2x)}$		25	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	-	25	35
Output Fall Time of Output Ports		t_{OF}		-	-	25	35
Data Clock Frequency		F_{DCLK}		-	-	-	25
Gray Scale Clock Frequency***		F_{GCLK}		-	-	-	20
2x Gray Scale Clock Frequency ***		$F_{GCLK, 2x}$		-	-	-	10

* Refer to the Timing Waveform, where n=0~7

** In timing of "Read Configuration", the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

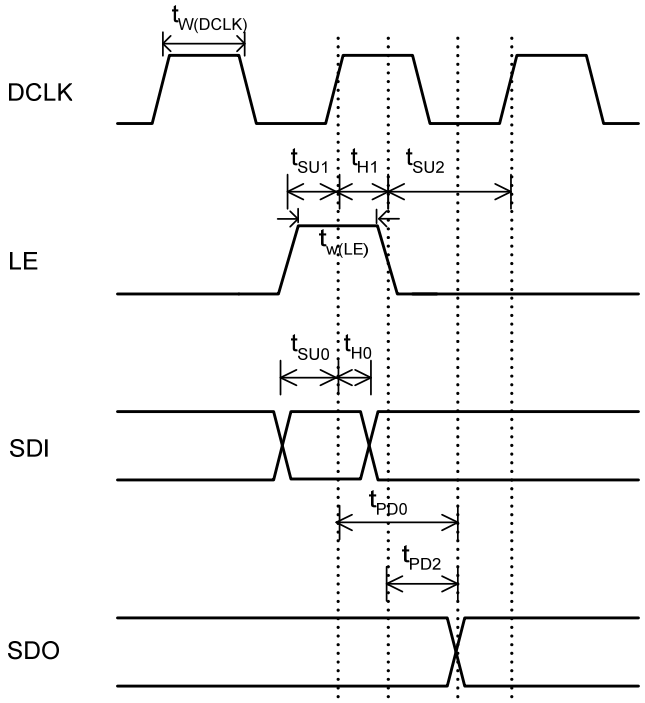
*** With uniform output current.

Test Circuit for Switching Characteristics

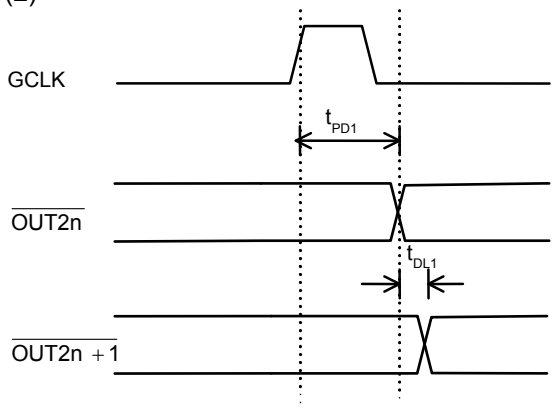


Timing Waveform

(1)



(2)



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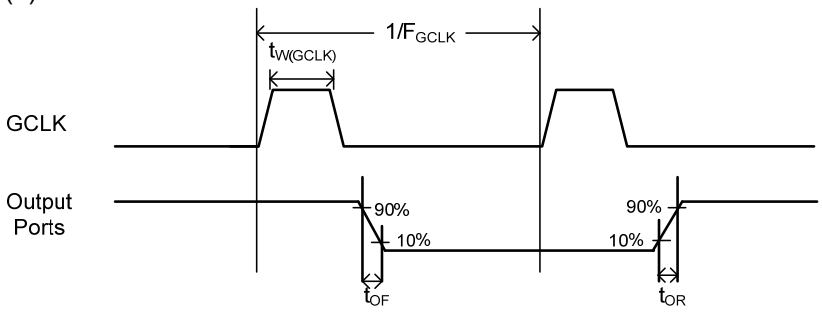
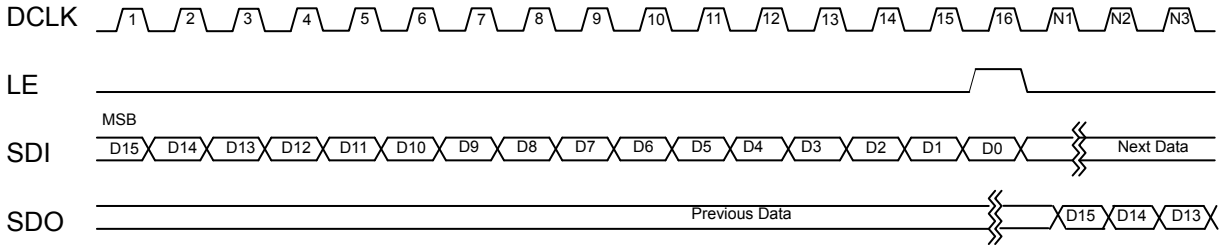


Principle of Operation

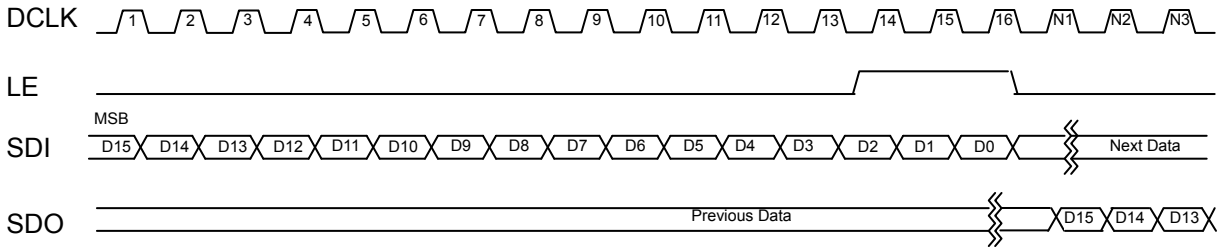
Control Command

	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**The Action after a Falling Edge of LE**
Data Latch	High	1	Serial data are transferred to the buffers
Global Latch	High	3	Buffer data are transferred to the comparators
Read Configuration	High	5	Move out “configuration register” to the shift registers
Write Configuration	High	11	Serial data are transferred to the “configuration register”
Enable Write Configuration	High	15	To enable “Write Configuration”

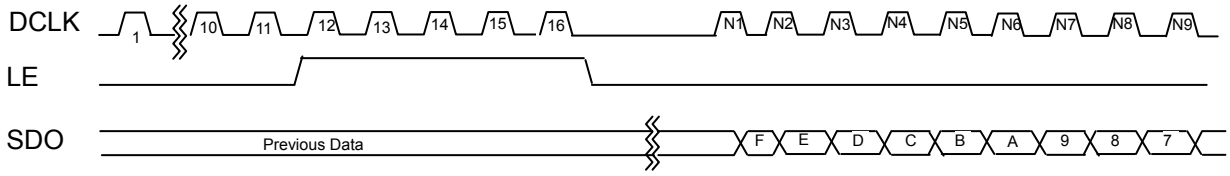
Data Latch



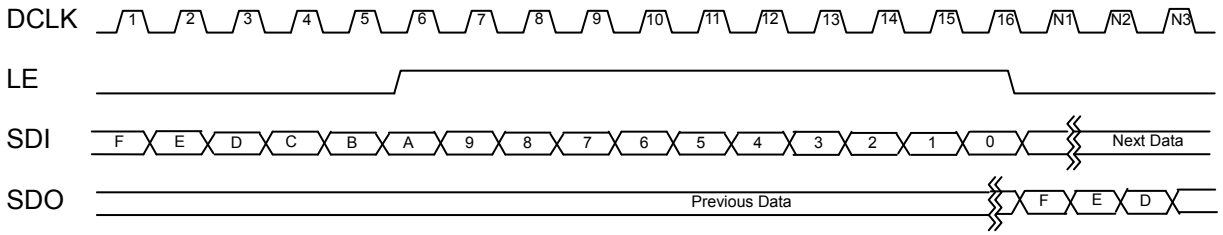
Global Latch



Read Configuration



Write Configuration

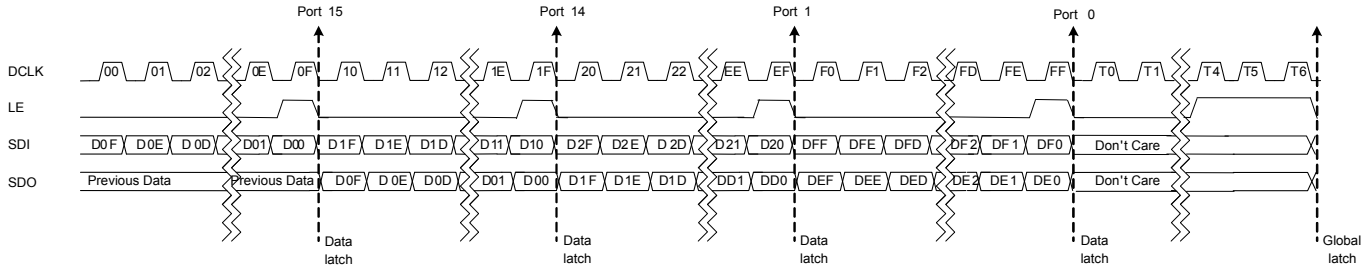


Setting Gray Scales of Pixels

MBI5043 implements the gray level of each output port using the S-PWM control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales.

The 16-bit input shift register latches 16 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for additional latch, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

Full Timing for Data Loading



Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

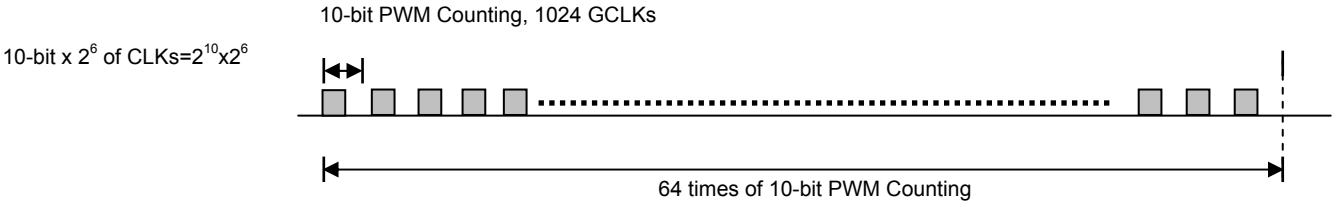
e.g.. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	6’b101011						0	0	0	0

Bit	Attribute	Definition	Value	Function
F~E	Read/Write	GCLK shift	00	00: shift 0 GCLK 01: shift 2 GCLK 10: shift 4 GCLK 11: shift 8 GCLK
D	Read	Reserved	0	Please keep “0”
C~B	Read/Write	Select pre-charge mode	00(Default)	00:Mode1 01:Mode2 10:Mode3 11:Mode4
A	Read/ Write	Color shift compensation [A]	0(default)	Color shift compensation [A,B] =[0,0]: disable Color shift compensation [A,B] =[0,1]: Mode1 Color shift compensation [A,B] =[1,0]: Mode2 Color shift compensation [A,B] =[1,1]: Mode3
9~4	Read/Write	Current gain adjustment	000000~ 111111	6’b101011 (Default, 100%) 000000:12.5% …. 111111:200%
3	Read/Write	GCLK rising/falling edge trigger	0	0: disable 1: enable
2	Read/Write	Color shift compensation [B]	0 (Default)	Color shift compensation [A,B] =[0,0]: disable Color shift compensation [A,B] =[0,1]: Mode1 Color shift compensation [A,B] =[1,0]: Mode2 Color shift compensation [A,B] =[1,1]: Mode3
1	Read	Reserved	0	Please keep “0”
0	Read/Write	Disable/Enable	0	0: disable 1: enable

The PWM Counting Mode

MBI5043 supports S-PWM, scrambled PWM, technology. With S-PWM , the total PWM cycles can be broken down into 64 times of 10-bit PWM counting to achieve overall same high bit resolution.



: Output ports are turned “on”.

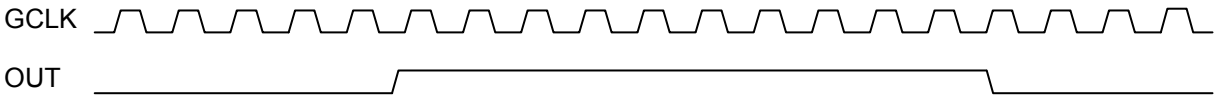
Synchronization for PWM Counting

MBI5043 updates the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5043 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.

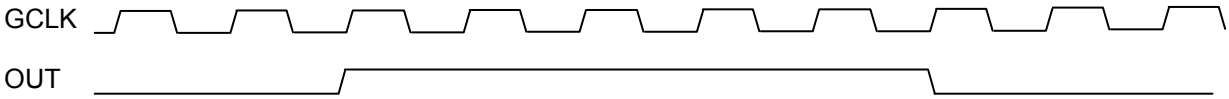
GCLK rising/falling edge trigger

Compared to output channel triggered by traditional rising edge, MBI5043 provides a feature in rising/falling edge trigger that can realize higher refresh rate at lower GCLK frequency to lower the impact of EMI. In rising/falling edge trigger mode, a 16-bit PWM cycle can be accomplished in 32,768 GCLK counts.

Rising edge trigger
GCLK=20Mhz, PWM=10



Rising/falling edge trigger
GCLK=10Mhz, PWM=10



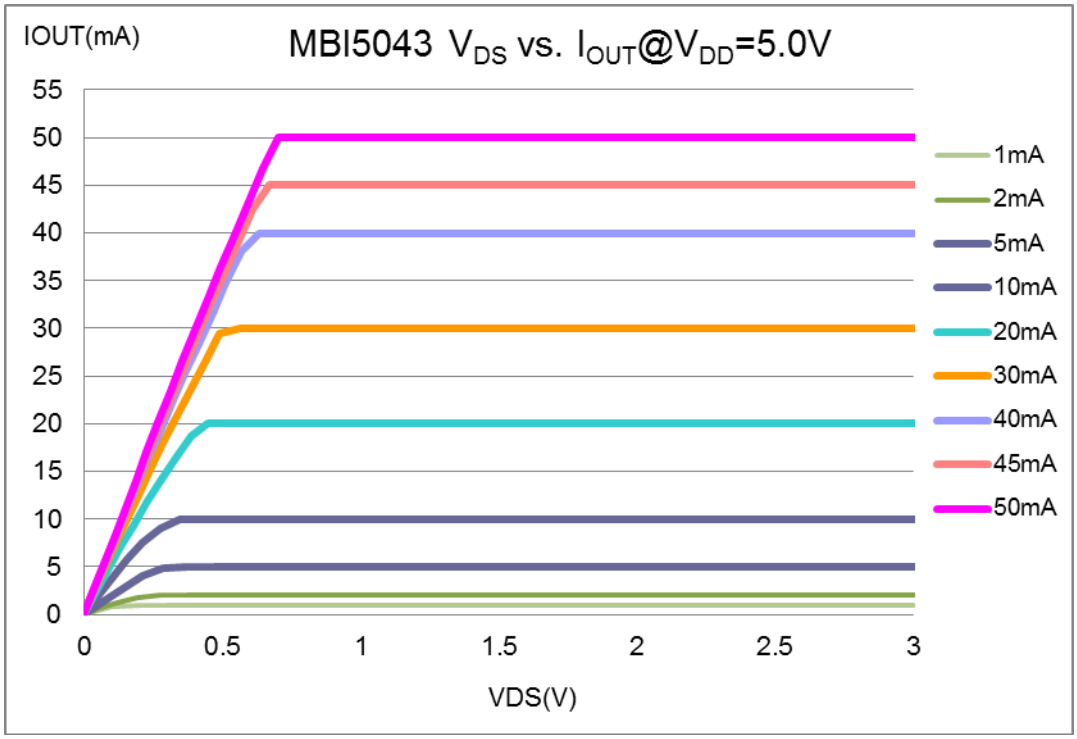
Please be noted, in rising/falling edge trigger mode, maximum GCLK frequency should be less 16.5Mhz to make sure of getting a uniform output because of t_{OR} and t_{OF} of output ports.

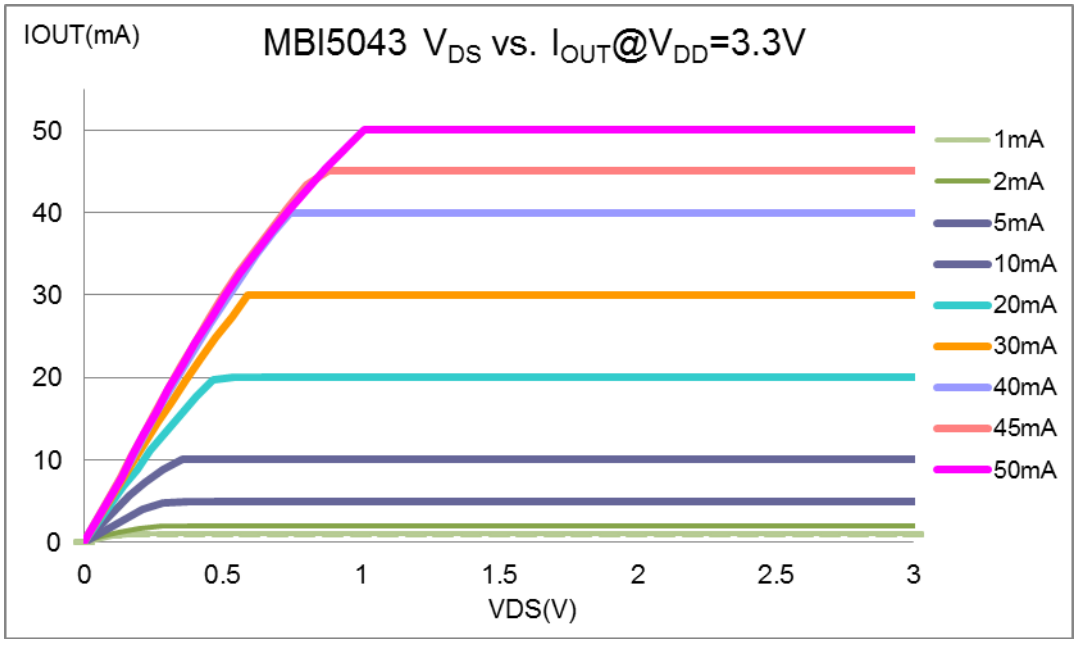
Constant Current

In LED display application, MBI5043 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 2.5%, and that between ICs is less than ±3.0%.

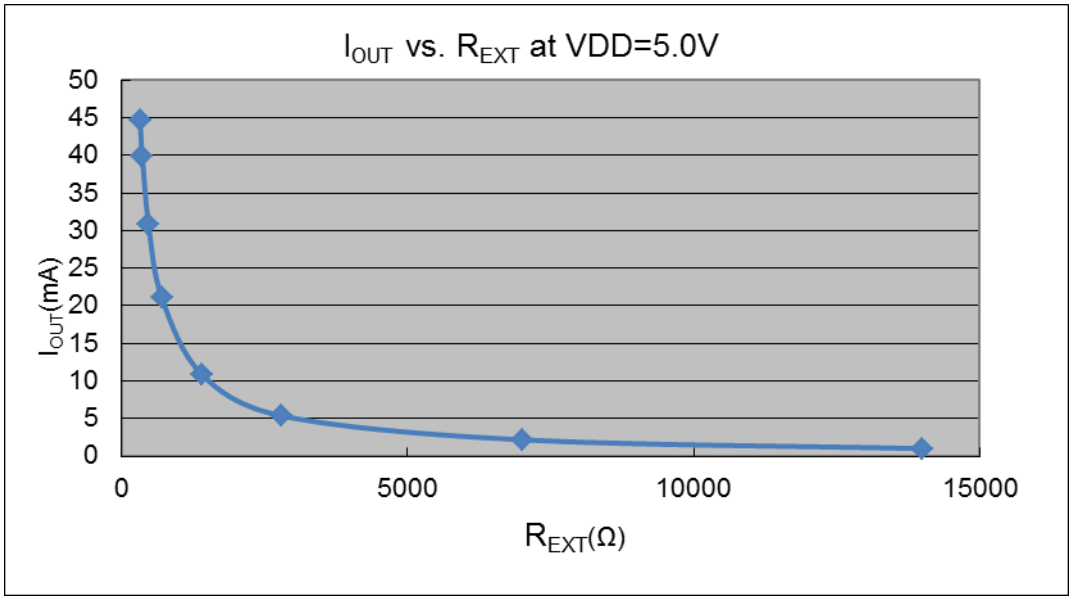
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

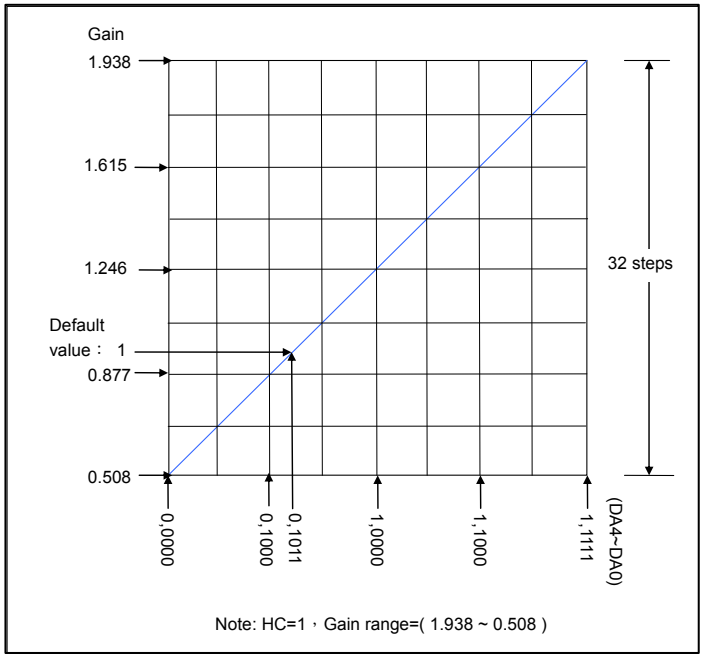


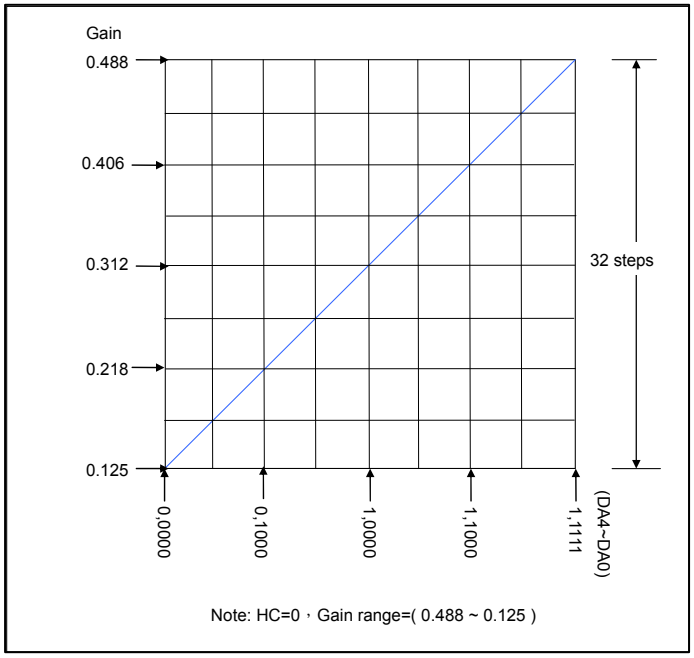
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.61Volt x G; I_{OUT}=($V_{R\text{-}EXT}$/R_{ext})x23

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit4 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=700Ω if G is set to default value The formula and setting for G are described in next section.

Current Gain Adjustment





The bit 9 to bit 4 of the configuration register set the gain of output current, i.e., G. As totally 6-bit in number, i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0	-	-	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 4 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

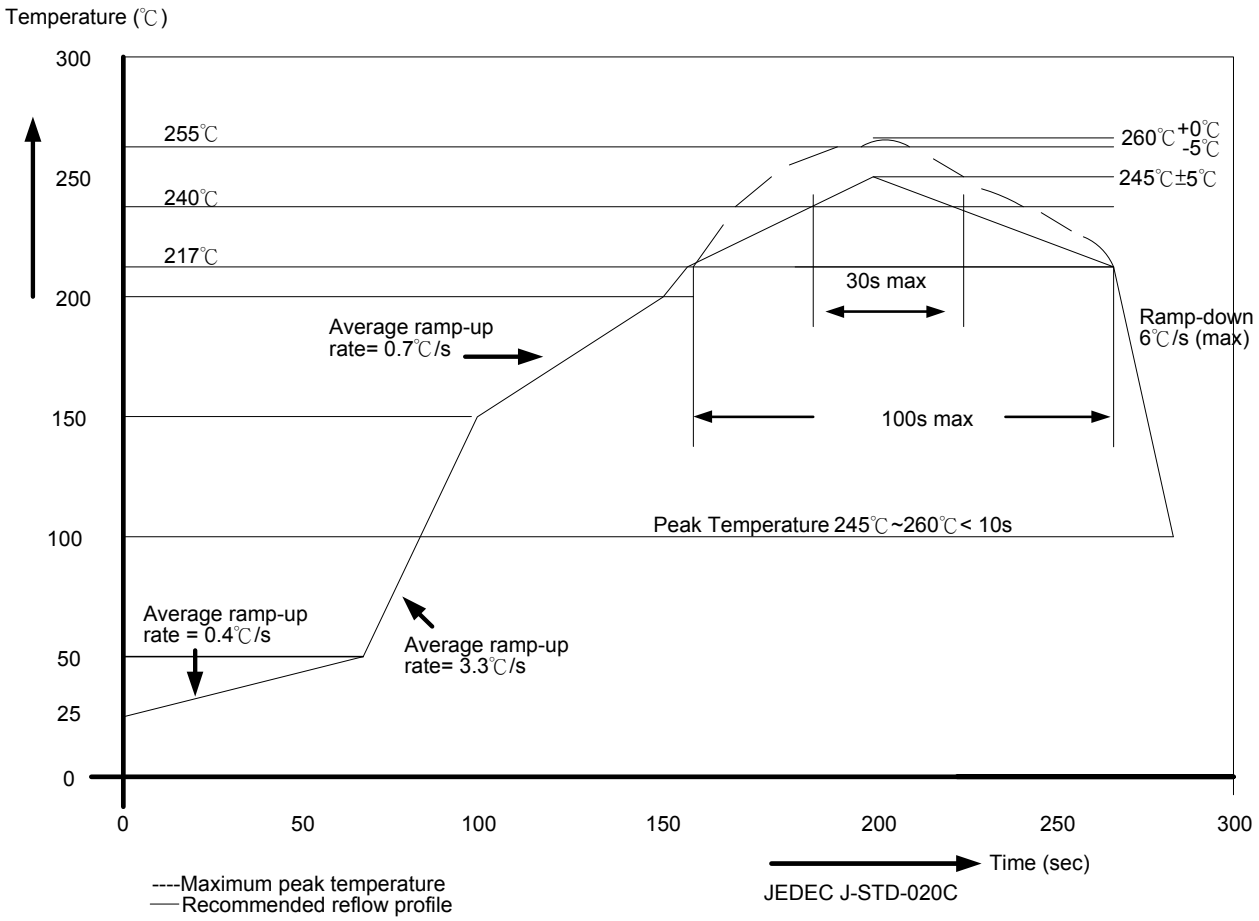
Staggered Delay of Output

MBI5043 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time among $\overline{OUT2n}$, and $\overline{OUT2n+1}$, by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green " to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 oC to 260oC for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

For managing MSL3 Package, it should refer to JEDEC J-STD-020C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

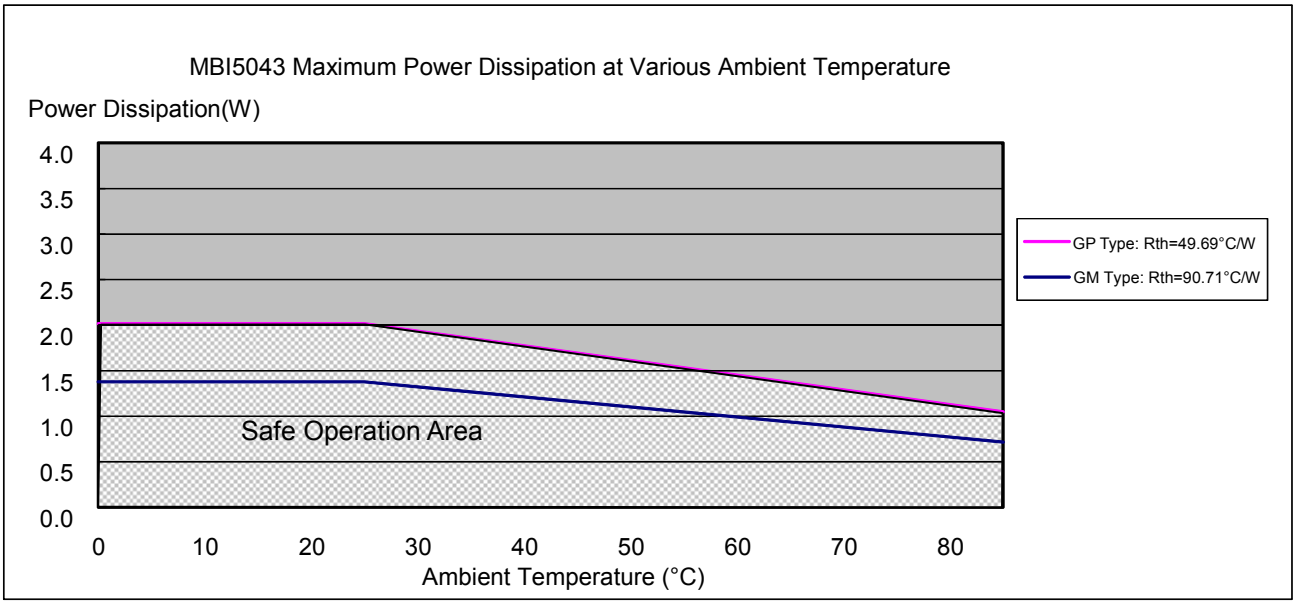
*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	62	1.6
GM	90.71	1.38

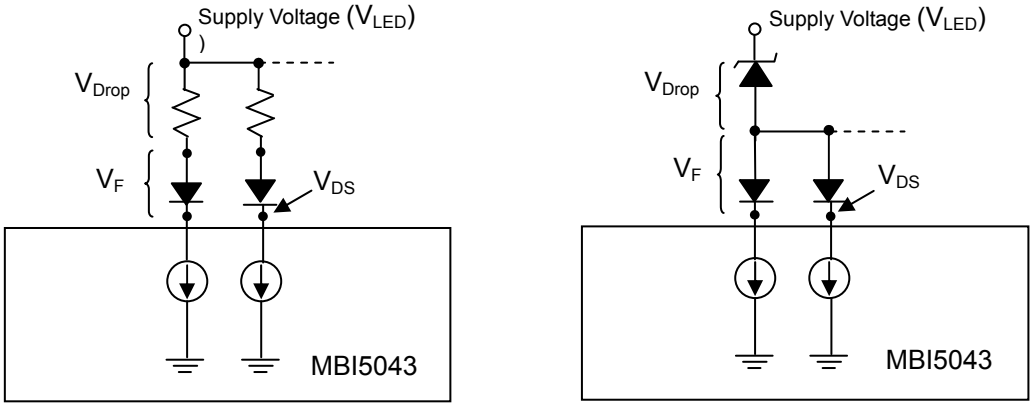


LED Supply Voltage (V_{LED})

MBI5043 are designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=2~45mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)}$ >$P_{D\ (max)}$ when V_{LED}=5V and V_{DS}=V_{LED}–V_F, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets V_{DS}=(V_{LED}–V_F)–V_{DROP}.

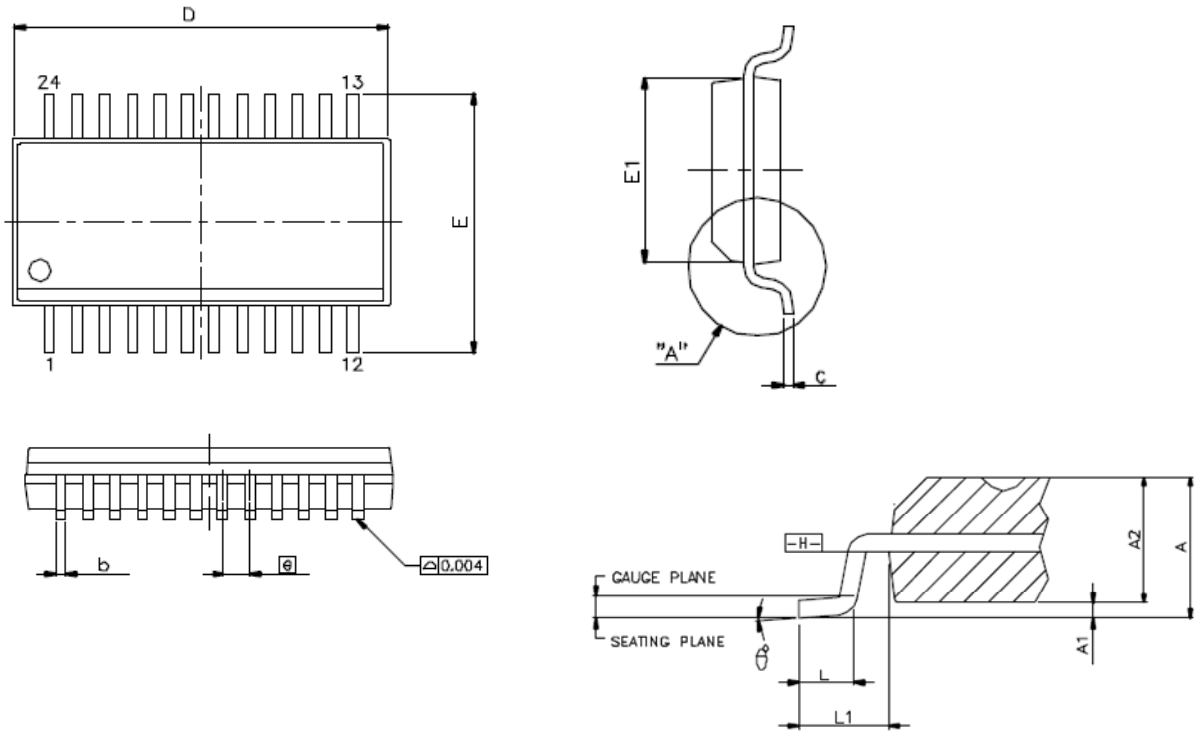
Resistors or Zener diode can be used in the applications as shown in the following figures.



Switching Noise Reduction

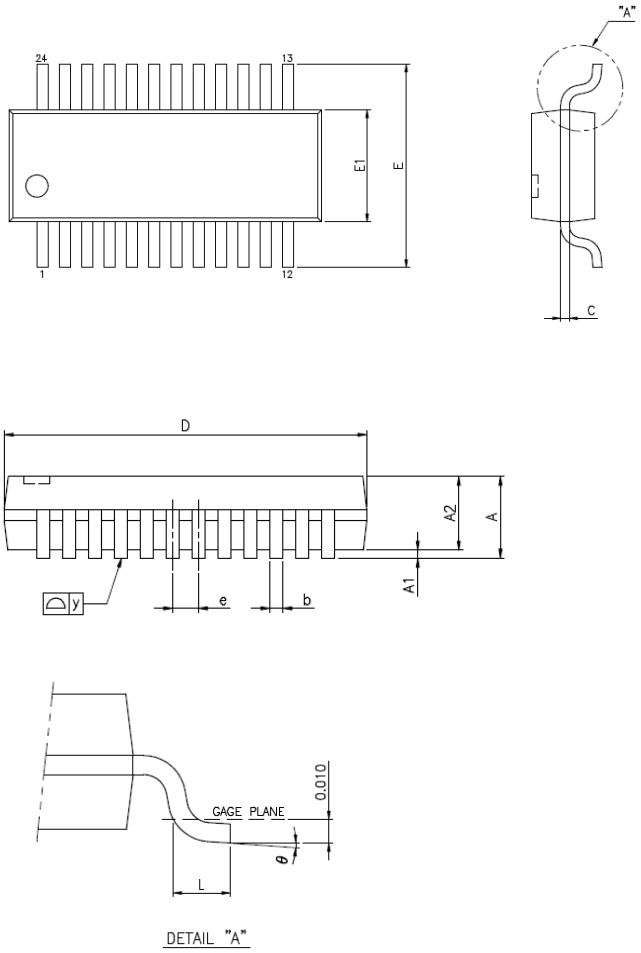
LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
Θ°	0	—	8	0	—	8

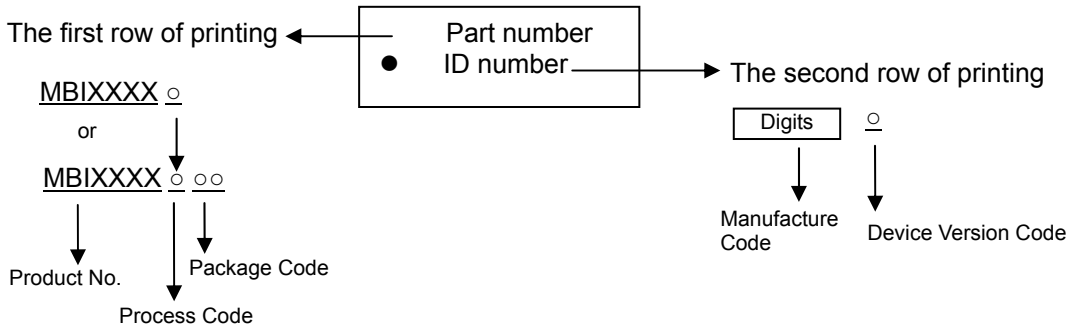
MBI5043GP Outline Drawing



SYMBOLS	DIMENSIONS SHOWN IN INCH			DIMENSIONS SHOWN IN MM		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.058	0.063	0.068	1.473	1.600	1.727
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	0.054	0.057	0.060	1.372	1.448	1.524
b	0.008	0.010	0.012	0.203	0.254	0.305
C	0.007	0.008	0.010	0.178	0.203	0.254
D	0.276	0.280	0.284	7.010	7.112	7.214
E	0.178	0.182	0.185	4.521	4.623	4.699
E1	0.096	0.100	0.103	2.438	2.540	2.616
e	–	0.020	–	–	0.508	–
L	0.016	0.025	0.050	0.406	0.635	1.270
y	–	–	0.003	–	–	0.076
Θ	0°	–	8°	0°	–	8°

MBI5043GM Outline Drawing

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
V1.00	A
V1.01	A

Product Ordering Information

Product Ordering Number*	"Pb-free & Green" Package Type	Weight (g)
MBI5043GP-A	SSOP24L-150-0.64	0.11
MBI5043GM-A	mSSOP24L-100-0.5	0.079

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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