LZC9150

Multi-Mode PWM Flyback Controller Integrated Enable Control

LOZEN TECNOLOGY INC

General Description

LZC9150 is a high performance current mode PWM controller which integrated primary side enable control. It provides functions of primary side enable control, low start up current, fast start up, multi-operation mode. Those features make it to achieve high efficiency and low standby power with effective system cost.

The LZC9150 integrated CCM, QR, GREEN, BURST multi operation mode. At heavy load, the IC operates in CCM mode. As load decrease, it operates in QR mode. At light load condition, the system operates in green mode for high efficiency. And at zero load, the IC will operate in BURST mode to enhance power saving.

The LZC9150 offers comprehensive protection to prevent the circuit from damage under abnormal conditions. Furthermore, the LZC9150 features frequency swapping and soft driving function to minimize the noise and improve EMI performance.

The LZC9150 is offered in SOP8 package.

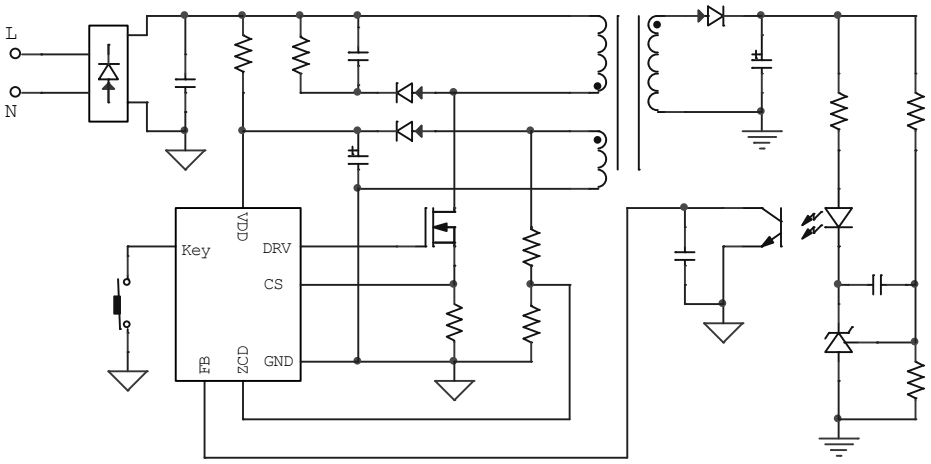
Features

- Primary side enable trigger control
- Internal Soft Start
- Multi-Mode Operation
  - CCM @ Heavy Load and Low Line
  - QR-Like Operation @ Medium Load
  - Green mode with Valley Skip @ Light Load
  - Burst Mode @ No Load
- VDD Over voltage protection
- Cycle by cycle current limit
- Second level over current protection
- Output over voltage protection (OVP)
- Output short protection (SCP)
- Over Load protection (OLP)
- Internal OTP

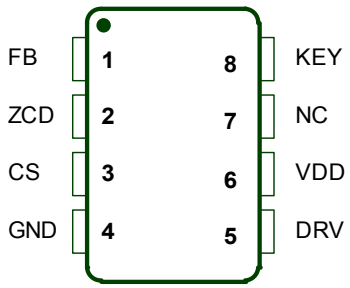
Applications

- Switching AC/DC power adapter
- Adapters/Chargers
- Industrial Power Systems

Typical Application



Pin Configuration（SOP8）



Absolute Maximum Ratings (Note 1)

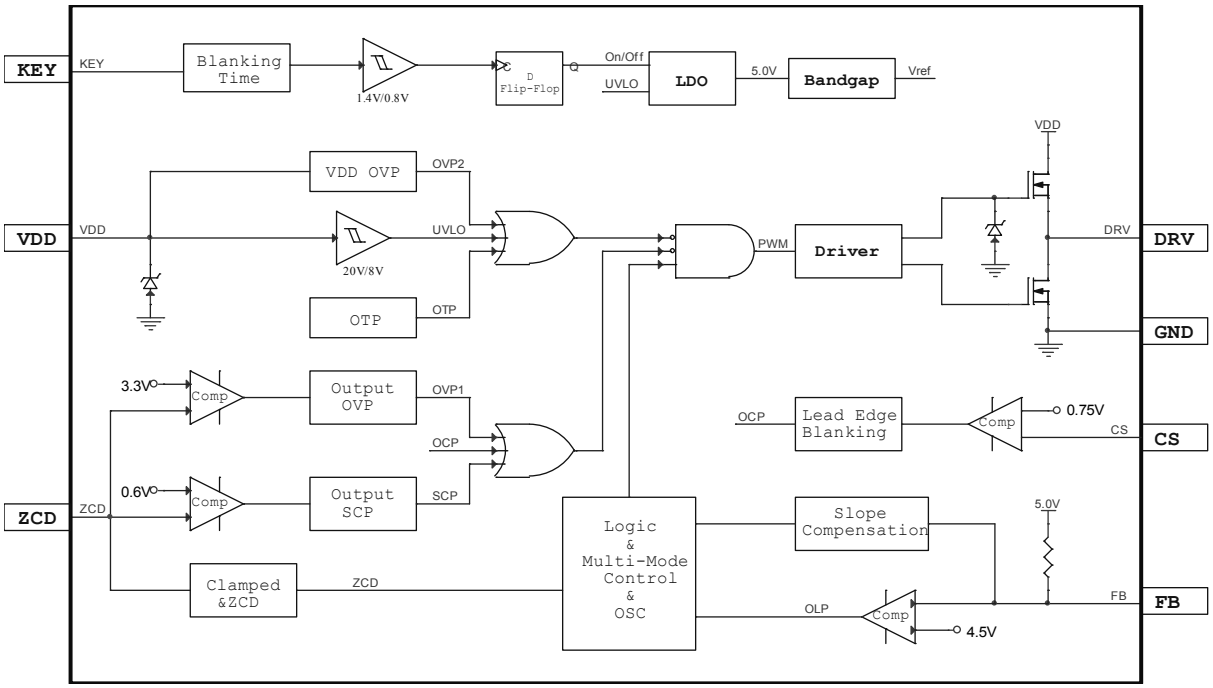
- Supply Input Voltage, VDD ---------- 30V
- Gate pin---------- 30V
- other Pins ---------- - 0.3V to 6.5V
- Package Thermal Resistance, θ_{JA}

  SOP8 ---------- 165℃ /W
- Junction Temperature ---------- 160℃
- Lead Temperature (Soldering, 10 sec.) ---------- 260℃
- Storage Temperature Range ---------- -55℃ to 150℃
- ESD Susceptibility (Note2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note3)

- Junction Temperature ---------- -40℃ to 125℃
- Ambient Temperature ---------- -40℃ to 85℃
- Supply Input Voltage, VDD ---------- 11V to 23V
- VDD capacitor ---------- 1uF to 3.3uF

Block Diagram



Pin Assignment

Name	I/O	Pin No.	Description
FB	I	1	Secondary side voltage feedback. The capacitor is placed between it and GND.
ZCD	I/O	2	Detect output diode zero current. Connected to a resistor divider for sensing the reflected voltage from auxiliary winding.
CS	I	3	Current sense pin, a resistor connects to sense the MOSFET current.
GND	POWER	4	Power Ground.
DRV	O	5	Totem-pole output to drive the external power MOSFET, Maximum Voltage is internally clamped to 16V.
VDD	POWER	6	Power Supply.
NC	/	7	No connect.
KEY	I/O	8	Enable trigger control pin, low voltage enables.

Electrical Characteristics

V_{DD}=15V, T_A=25℃, unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Supply Voltage (VDD Pin)						
VDD_{ON}	UVLO ON			14.2		V
VDD_{OFF}	UVLO OFF			8		V
VDD_{CLP}	VDD Clamp voltage	Key no trigger		19.6		V
VDD_{HOLDH}	VDD holding exit voltage			10		V
VDD_{HOLDL}	VDD holding enter voltage			9		V
VDD_{OVP}	VDD OVP voltage			28		V
I_{ST_1}	Startup current	VDD ≤ 14.2V		1		uA
I_{ST_2}	Startup current	VDD > 14.2V		30		uA
I_{SS_OP}	Normal operation current	FB floating		500		uA
I_{SS_BST}	Burst Mode operation current	FB=0V		400		uA
Voltage Feedback (FB Pin)						
V_{FB_OPEN}	FB open voltage	FB floating		5.12		V
R_{FB}	FB pull up resistor			25		KΩ
V_{FB_GREEN}	Green mode threshold			2.1		V
V_{FB_BSTH}	Exit burst mode threshold			1.3		V
V_{FB_BSTL}	Enter burst mode threshold			1.2		V
V_{FB_OLP}	Over Load protection threshold			4.55		V
T_{FB_OLP}	Over Load protection de-bounce time			280		ms
Current sense (CS Pin)						
V_{CS_MAX}	Cycle by cycle current limit	0.7V<ZCD<3.3V		0.75		V
V_{CS_SEC}	Second CS voltage limit state			1.4		V

V_{CS_MIN}	Minimum CS voltage limit			183		mV
T_{SS}	Soft start period			8		mS
I_{LINE}	Line compensation current (Internal line compensation)	ZCD source current=1mA		0.25		V
T_{LEB}	Lead edge time			330		nS
Zero current detection (ZCD Pin)						
V_{ZCDH}	High clamp voltage of ZCD	Sink current 1mA		6		V
V_{ZCDL}	Low clamp voltage of ZCD	Source current 1mA		0		V
V_{SCP}	Output short voltage detection			0.6		V
T_{SCP}	SCP debounce time			10		ms
V_{OVP}	Output over voltage threshold			3.3		V
Enable trigger control pin **(Key Pin)**						
V_{KEYH}	Release Voltage		1.4			V
V_{ZCDL}	Trigger Voltage				0.8	V
I_{KEY}	Short Current			5		uA
T_{LEB_KEY}	Blanking time			120		mS
Oscillator						
F_{OSC}	CCM Frequency			71		KHz
F_{BURST}	Burst Frequency			25		KHz
D_{MAX}	Maximum duty cycle			80		%
T_{ONMAX}	Maximum Ton time			12		uS
Internal OTP						
OTP_H	OTP Temperature			150		℃
OTP_{HYS}	OTP Hysteresis			30		℃
GATE Driver (DRV Pin)						
T_R	DRV rising time	C_{GATE}=1nF		100		ns
T_F	DRV falling time	C_{GATE}=1nF		50		ns

V_{GCLAMP}	DRV Clamping voltage			16		V

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Operation

LZC9150 is a high performance current mode PWM controller which integrated primary side enable control. It provides functions of primary side enable control, low startup current, fast startup, multi operation mode. Those features make it to achieve high efficiency and low standby power with effective system cost. Its major features are described as below.

Startup Current

The typical start-up current is 1uA. Very low start-up current allows the LZC9150 to increase the value of start-up resistor and then reduce the power dissipation on it.

Under Voltage Lockout (UVLO) and KEY Enable

A hysteresis UVLO comparator is implemented in LZC9150, then the turn-on and turn-off thresholds level are fixed at 14.2V and 8V respectively. After the VDD voltage reaches 14.2V, wait for the KEY button to be valid. During this period, the VDD clamp voltage is 19.6V. KEY to maintain low level over 120mS, that a valid start signal. This hysteresis shown in Fig1 ensures that the start-up capacitor will be adequate to supply the chip during start-up.

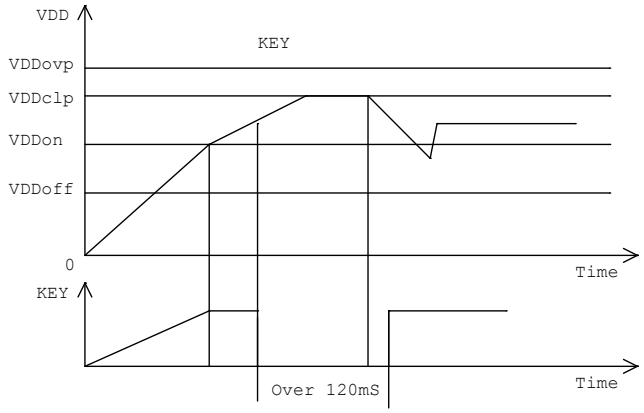


Fig 1 VDD Start Up

Multi-Mode Operation

LZC9150 is a multi-mode QR/CCM controller. The controller changes the mode of operation according to VFB pin voltage. At the normal operating condition, the IC operates in CCM mode. Thus, small size transformer can be used with high power conversion efficiency.

As the output load current is decreased, the IC operates in QR mode to reduce the switching loss. In the QR mode, the frequency varies depending on the line voltage and the load conditions.

When output load continue decreased, the IC will enter GREEN MODE for high power conversion efficiency. The max switching frequency clamp will start to linearly decrease from 67kHz to 23kHz. The valley switching characteristic is still preserved in green mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced.

At no load or very light load conditions, switching loss of MOSFET is the main power dissipation. The LZC9150 enters BURST MODE control and the gate output driver will be disabled immediately if VFB

drops below V_{FB_BSTL}. When VFB rise back to V_{FB_BSTH}, the gate output driver again. Otherwise, the gate will remains at off state to enhance power saving.

Soft Start

The LZC9150 integrated an internal 1~8ms soft start function during system power on period.

Zero Current Detection (ZCD)

The ZCD will detect auxiliary winding voltage to turn on the MOSFET. The block generates a MOSFET turn-on signal as the inductor current reaches zero value.

Leading-edge Time(LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense resistor. To avoid fault trigger, a leading-edge time is built in. During this period, the current-limit comparator is disabled and cannot switch off the gate driver.

Internal Slope Compensation

A built-in slope compensation circuit is constructed in LZC9150. When the switch is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

VDD Holding

In order to avoid the VDD UVLO in burst mode operation, the LZC9150 build in the VDD Holding function. When LZC9150 stop output gate pulse in burst mode, VDD will continue decreasing. And LZC9150 will output gate pulse if VDD drop below VDD_{HOLDL} value. This state will release after VDD reach VDD_{HOLDH} value.

VDD over Voltage Protection (OVP) –Auto recovery

When the VDD voltage is higher than the OVP threshold voltage, the output gate driver circuit will be shut down immediately to stop the switching of power MOSFET.

The VDD OVP function is an auto-recovery type protection. If OVP happens, the pulses will be stopped and recover at the next UVLO on.

Output OVP -- Auto recovery

An output over voltage protection is implemented in the LZC9150. It senses the auxiliary voltage via the divided resistors. The overvoltage protection works by sampling the ZCD Pin voltage after a delay time. The sampling voltage level is compared with internal threshold voltage 3.3V. If the sampling voltage exceeds the OVP threshold value, LZC9150 switches the power MOSFET off.

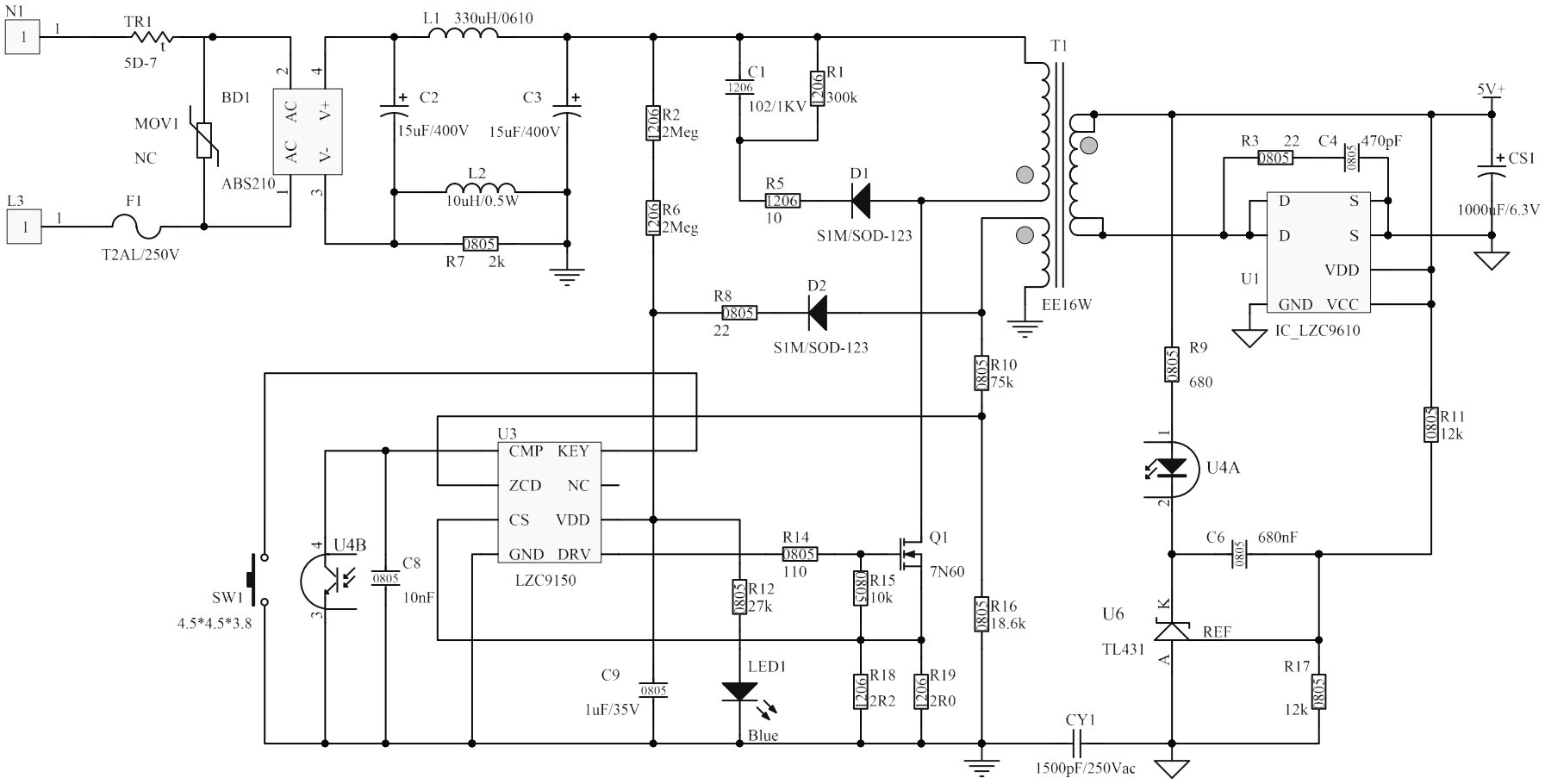
Output SCP -- Auto recovery and Latch optional

An output short circuit protection is implemented in the LZC9150. It senses the auxiliary voltage via the divided resistors. If the ZCD voltage declines below 0.6V for over the 10ms, the protection will be activated to turn off the gate.

Over Load protection (OLP) -- Auto recovery and Latch optional

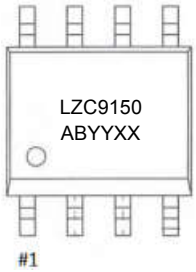
An over load protection is implemented in the LZC9150. When VFB input voltage exceeds the OLP threshold voltage 4.55V for more than T_{FB_OLP}, the protection will be activated to turn off the gate.

Reference Application Schematic



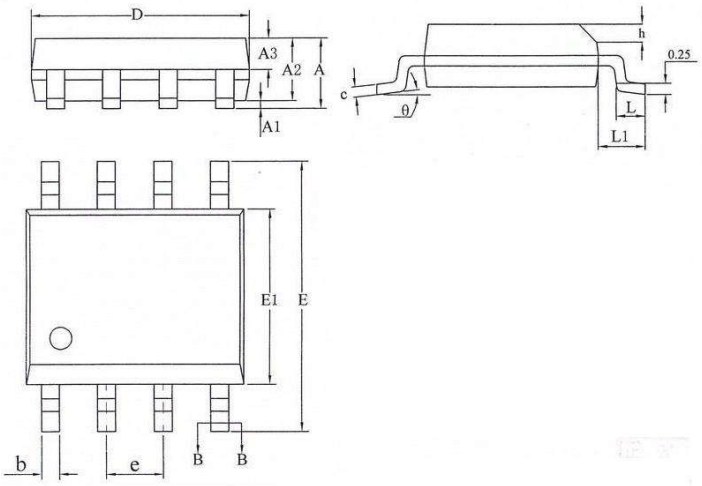
Ordering & Marking Information

Device Name: LZC9150 for SOT23-6



LZC9150
ABYYXX: AB for Assembly house，YYXX for Date code

Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°

Compliant to JEDEC Standard MS12F
Controlling dimensions are in inches; millimeter dimensions are for reference only
This product is RoHS compliant and Halide free.
Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270°C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.25 mm per side. D and E1 dimensions are determined at datum H. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outer most extremes of the plastic boxy exclusive of mold flash, tie bar burrs, gate burrs and inter-lead flash, but including any mismatch between the top and bottom of the plastic body.